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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,937	09/12/2003	Andrew M. Spencer	200208963-1	8405
22879	7590	05/15/2006	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			ABRAHAM, ESAW T	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/661,937	SPENCER ET AL.
	Examiner Esaw T. Abraham	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 12 September 2003.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-24 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) 25-33 are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 12 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. 05/02/06

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## **DETAILED ACTION**

### **Election / Restriction**

Restriction to one of the following invention is required under 35 U.S.C. 121

I. Claims 1-24, drawn to:

(a) A device comprising a memory array in which a plurality of codewords is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data and an error code correction module coupled to a memory array wherein when multiple units of data are to be read from the device for an address a codeword stored in a location associated with the address is fetched from the memory array, the error code correction module decodes the codeword and corrects any errors in the data block for that codeword, and the multiple units of data are read from the corrected data block (as in claim 1); (b) A device comprising a memory array in which a plurality of codeword is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data and an error code correction module coupled to a memory array wherein when multiple units of data are to be written to the device for an address, the multiple units of data are encoded together to generate a codeword and the generated codeword to the memory in a location associated with the address (as in claim 8); (c) The method of reading one or more units of data from a memory array in which

a plurality of codeword is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data, the method comprising when multiple units of data are to be read from memory array for an address, fetching the codeword stored in a location associated with the address from the memory array, decoding the codeword and correcting any errors in the data block for the codeword and reading the multiple units of data from the corrected data block (as in claim 16); (d) A method of writing on or more units of data to a memory array in which a plurality of codeword is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data the method comprising when multiple units of data are to be written to the memory array for an address encoding the multiple units of data together to generate a codeword and writing the generated codeword to the memory array in the location associated with the address (as in claim 22) classified in 714/768.

II. Claims 25-31, drawn to:

a) A system, comprising: an assisted memory in which a plurality of codeword is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and a second device coupled to the assisted memory; wherein when the second device attempts to read multiple units of data from the assisted memory for an address, a codeword stored in a location associated with the address is

fetched from the assisted memory, the codeword is decoded, any errors in the data block are corrected for that codeword, and the multiple units of data are read from the corrected data block and supplied to the second device, b) A system, comprising: assisted memory in which a plurality of codeword is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and a second device coupled to the assisted memory; wherein when the second device attempts to write multiple units of data to the assisted memory for an address, the multiple units of data are encoded together to generate a codeword and the generated codeword is written to the assisted memory in a location associated with the address are classified in 714/763.

III. Claim 32, drawn to:

A device, comprising: a means for receiving an address, a means for fetching a codeword stored at a location associated with the address, wherein the codeword comprises a parity block and a data block that comprises a plurality of units of data; a means for decoding the codeword and correcting any errors in the data block for that codeword', and a means for reading multiple units of data from the corrected data block classified in 714/758.

IV. Claim 33, drawn to:

A device, comprising: a means for receiving an address; a means for receiving multiple units of data for the address, a means for encoding the

multiple units of data together to generate a codeword, wherein the codeword comprises a data block comprising a plurality of units of data and a parity block generated from the data block; and a means for storing the generated codeword at a location associated with the address classified in 714/805.

The invention are distinct, each from the other because of the following reasons: Invention Group I, Group II, Group III, and group IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable.

In the instance case, invention Group I has separate utility separate utility such as multiple units of data are to be read from the device for an address a codeword stored in a location associated with the address is fetched from the memory array, the error code correction module decodes the codeword and corrects any errors in the data block for that codeword, and the multiple units of data are read from the corrected data block.

In the instance case, invention Group II has separate utility separate utility such as an assisted memory in which a plurality of codeword is stored, each codeword comprising an error correction code and a data block comprising a plurality of units of data; and a second device coupled to the assisted memory; wherein when the second device attempts to read multiple units of data from the assisted memory for an address, a codeword stored in a location associated with the address is fetched from the assisted memory, the codeword is decoded.

In the instance case, invention Group III has separate utility separate utility such as a means for receiving an address, a means for fetching a codeword stored at a location associated with the address, wherein the codeword comprises a parity block and a data block that comprises a plurality of units of data; a means for decoding the codeword and correcting any errors in the data block for that codeword, and a means for reading multiple units of data from the corrected data block.

In the instance case, invention Group IV has separate utility separate utility such as a means for receiving an address; a means for receiving multiple units of data for the address, a means for encoding the multiple units of data together to generate a codeword, wherein the codeword comprises a data block comprising a plurality of units of data and a parity block generated from the data block; and a means for storing the generated codeword at a location associated with the address. See MPEP 806.05(d).

Because these inventions are distinct for the reason given above and the search required for Group I is not required for Group II, III, IV, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group II is not for Group I, III, IV, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group III is not for Group I, II, IV, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group IV is not for Group I, II, III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Augustus Winfield on 02 May 2006 a provisional election was made with out traverse to prosecute the invention of Group I, claims 1-24.

Affirmation of the election must be made by applicant in replying to this office action. Claims 25-33 are withdrawn from further consideration by the examiner 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the specification. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

#### ***DETAILED ACTION***

1. Claims 1-24 are presented for examination.

***Specification***

2.
  - a) The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
  - b) The title of "Assisted memory device" is so broad as to not provide any description of the inventive concept to which the claims are directed. A new title is required that is clearly indicative of the invention.

***Claim objections***

3. Claims **1-2, 7-10, 16-18 and 20-24** are objected to because of the following informalities:

Claim 1 recites, "A device" in the preamble. CFR § 1.75 states that the specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention or discovery. A method does not indicate what a subject matter the claims are directed to.

- a) Please change the phrase "are to be read" to ---are read--- (see claim 1, line 6).
  - b) Please change the phrase "is to be read" to ---is read--- (see claim 2, lines 1 and 5).
  - c) Please change the phrase "are to be read" to ---are read--- (see claim 7, line 2).

- d) Please change the phrase "are to be read" to ---are read--- (see claim 8, line 6).
- e) Please change the phrase "to be written" to ---written--- (see claim 9, lines 2, 4).
- f) Please change the phrase "to be written" to ---written--- (see claim 10, line 1).
- g) Please change the phrase "to be written" to ---written--- (see claim 16, line 4).
- h) Please change the phrase "to be read" to ---read--- (see claim 17, lines 2 and 7).
- i) Please change the phrase "to be performed" to ---performed--- (see claim 18, line 2).
- j) Please change the phrase "to be written" to ---written--- (see claim 20, lines 1, 2 and 4).
- k) Please change the phrase "to be written" to ---written--- (see claim 21, lines 2 and 4).
- l) Please change the phrase "to be written" to ---written--- (see claim 22, line 4).
- m) Please change the phrase "to be written" to ---written--- (see claim 23, lines 1, 2 and 4).
- n) Please change the phrase "to be written" to ---written--- (see claim 24, line 2).

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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4. **Claim 2** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 2, lines 4 and 5 "the single unit" does not have a clear antecedent basis.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-24** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Jeddelloh (U.S. PN: 6,076,182).

**As per claims 1 and 16:**

Jeddelloh substantially teaches a system and method for storing data subject to memory error, divides each data word into a plurality of sub-words and creates a separate error correction code for each of the sub-words. The system includes a plurality of error correction modules, each performing error correction on a separate sub-word of the data word whereby the data word is divided into four quarter words and a separate error correction code is created for each of the four quarter words (see col. 2, lines 20-36). Jeddelloh teaches that the system includes a memory controller (18) that controls the manner in which data is written to and read from the memory bank (14) of the memory module (12). The memory controller (18) interfaces the

memory module 12 with a computer processor (20) via a processor bus (22). The processor bus (22) includes data, control, and address buses 24, 26, 28, that provide communication between the memory controller (18) and the processor 20 in a well-known manner (see col. 3, lines 22-32). Jeddelloh further teaches a memory controller (18) includes a processor (54), an address decoder 56, and a data buffer 57 that enable the controller 18 to respond to requests or access to the memory module 12 from the processor 20 or bus agent 38 via the processor bus (22) and furthermore the address decoder stores a definition of the address boundaries for the memory bank and any other memory banks of the memory module (12). The data buffer (57) temporarily stores each data word requested to be written to memory module (12) and each data word read from the memory module (12) (see col. 3, lines 33-48).

**As per claims 2-5:**

The claims are rejected under similar rationale as set forth in claim 1 including Jeddelloh teaches data buffer (57) temporarily stores each data word requested to be written to memory module (12) and each data word read from the memory module (12) (see col. 3, lines 33-48).

**As per claims 7-8:**

The claims are rejected under similar rationale as set forth in claim 1 including Jeddelloh teaches that dividing each data word into a plurality of sub-words and creates a separate error correction code for each of the sub-words. Each of the error correction codes includes a plurality of check bits with check bit values based on the data bit values of the corresponding sub-word of the data word (see col. 2, lines 20-36).

**As per claims 8, 12 and 22:**

Jeddeloh substantially teaches a system and method for storing data subject to memory error, divides each data word into a plurality of sub-words and creates a separate error correction code for each of the sub-words. The system includes a plurality of error correction modules, each performing error correction on a separate sub-word of the data word whereby the data word is divided into four quarter words and a separate error correction code is created for each of the four quarter words (see col. 2, lines 20-36). Jeddeloh teaches that the system includes a memory controller (18) that controls the manner in which data is written to and read from the memory bank (14) of the memory module (12). The memory controller (18) interfaces the memory module 12 with a computer processor (20) via a processor bus (22). The processor bus (22) includes data, control, and address buses 24, 26, 28, that provide communication between the memory controller (18) and the processor 20 in a well-known manner (see col. 3, lines 22-32). Jeddeloh further teaches a memory controller (18) includes a processor (54), an address decoder 56, and a data buffer 57 that enable the controller 18 to respond to requests or access to the memory module 12 from the processor 20 or bus agent 38 via the processor bus (22) and furthermore the address decoder stores a definition of the address boundaries for the memory bank and any other memory banks of the memory module (12). The data buffer (57) temporarily stores each data word requested to be written to memory module (12) and each data word read from the memory module (12) (see col. 3, lines 33-48).

**As per claims 9-11 and 14:**

The claims are rejected under similar rationale as set forth in claim 8 including Jeddeloh teaches an address decoder 56 stores a table that includes an indication of which memory addresses are associated with a memory bank 14. That is, the address decoder 56 stores a definition of the address boundaries for the memory bank 14 and any other memory banks of the memory module 12 (see col. 4, lines 4-13).

**As per claim 13:**

The claims are rejected under similar rationale as set forth in claim 8 including Jeddeloh teaches a memory controller 18 that controls the manner in which data is written to and read from the memory bank 14 of the memory module 12 (see col. 3, lines 33-35).

**As per claim 15:**

The claim is rejected under similar rationale as set forth in claim 8.

**As per claims 17-21:**

The claims are rejected under similar rationale as set forth in claim 16 including Jeddeloh teaches an address decoder 56 stores a table that includes an indication of which memory addresses are associated with a memory bank (14). That is, the address decoder (56) stores a definition of the address boundaries for the memory bank (14) and any other memory banks of the memory module (12) (see col. 4, lines 4-13).

**As per claims 23-24:**

The claims are rejected under similar rationale as set forth in claim 22 including Jeddeloh teaches an address decoder 56 stores a table that includes an indication of

which memory addresses are associated with a memory bank (14). That is, the address decoder (56) stores a definition of the address boundaries for the memory bank (14) and any other memory banks of the memory module (12) (see col. 4, lines 4-13) and furthermore, Jeddelloh teaches a memory controller (18) that controls the manner in which data is written to and read from the memory bank 14 of the memory module 12 (see col. 3, lines 33-35).

### **Conclusion**

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,848,070 Kumar, Harsh

US PN: 6,961,877 Si et al.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more

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information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*Esaw Abraham*

Esaw Abraham

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GUY LAMAPRE  
PRIMARY EXAMINER